

Simulation of Georgia Tech's CMOS Baseline Using T-SUPREM4 and MEDICI

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The Microelectronics Research Center of Georgia Tech has established silicon CMOS processing baselines as an important part of its research Platform that provides supports to research communities around the world for research into numerous devices and fabrication techniques. Successful process runs include 1 μ m double polysilicon and double metal CMOS, 2 μ m double polysilicon and double metal CMOS, 2 μ m single polysilicon and single metal CMOS, and other CMOS based devices. This paper seeks to outline the simulation model for CMOS and NMOS designs. It includes a process simulator, TSUPREM-4, which was utilized to represent the process run parameters for the devices and a device simulator, MEDICI, which was employed to extract electrical characteristics. The simulation model has been utilized to observe general relationships between several processing parameters, such as the P+ and N+ doping concentrations as well as Ion Implantation energies and dosages, and corresponding threshold voltage variations.

1. INTRODUCTION

Microelectronic device manufacture encompasses the fabrication, testing and simulation, of structures utilized in a variety of application specific integrated circuits. The fabrication of transistors, traditionally from elemental silicon wafers is conducted in a clean room environment utilizing various types of equipment. Process simulation is a critical element in facilitating the optimization of fabrication stages, confirming test results and theoretical models and providing physical insight into structural operation. TSUPREM-4 and SPEEDIE are two process simulators. Each phase of device manufacture is replicated to a high degree of accuracy.

Process simulation output includes two and three-dimensional structure profiles, and the extraction of structural and electrical parameters. Structural information includes doping profiles, impurity concentrations, and layer thickness whereas electrical extraction includes current vectors, electron, hole and potential concentrations. Majority charge carrier devices: junction field effect transistor JFET, metal semiconductor field effect transistor MESFET, the metal oxide semiconductor field effect transistor MOSFET and minority charge carrier devices: the p-n junction, n-p-n bipolar transistor and the p-n-p-n thyristor are typical device structures that can be simulated [1].

Device simulation can be used to replicate processing steps as well as analyzing the behavior of the finished structure under a multitude of biasing conditions. Results are categorized as models or characterization. MEDICI and PISCES are two device simulators. Device models are

imported into circuit simulations and characteristics extracted under various biasing conditions. Circuit simulators, SPICE, can be used to optimize IC designs. In general, process and device simulators utilize finite difference and finite element methods for analyzing basic semiconductor equations: The Poisson equation, equation of continuity for holes and electrons and current density equations.

2. CMOS Process Simulation

A. The CMOS Inverter

The CMOS processing baseline at the Georgia Institute of Technology Microelectronics Research Center engages in the fabrication of a variety of transistor structures supporting the research being conducted in application specific integrated circuits for related research disciplines. Previous process runs include: 20 μ m N-Channel MOSFET; 2 μ m P-well single metal single poly-silicon CMOS inverter and a 2 μ m N-well double metal double poly-silicon CMOS inverter. Supported research projects include multi channel chemical sensor array, MEMS, gate stack engineering and shallow junction CMOS [2].

CMOS circuits have revolutionized the electronics industry by producing fast switching low power circuit elements for use in watches, pacemakers and automobile clocks. The basic element of the circuit is the CMOS inverter. The inverter is composed of a P-Channel and N-Channel transistor connected to each other in series as a complementary pair. Input to the device is supplied at the gate terminals of both devices. The supply terminal is connected to the source of one transistor while the source of the other remains grounded. Output from the device is obtained from the mutual drain current flowing through both transistors, Figure 1

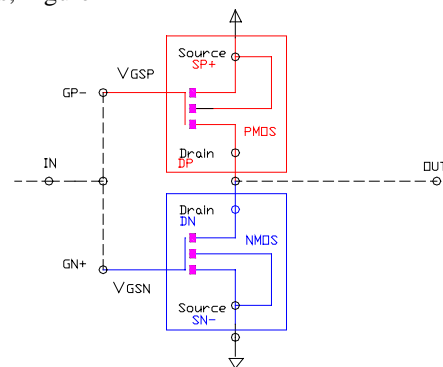


Figure 1. Basic CMOS Inverter Circuit Elements

B. Simulation Techniques

Process simulators provide quantitative and qualitative information regarding the relationship between final device characteristics and the fabrication parameters. TSUPREM-4, developed by Technology Modeling Associates and Stanford University Process Engineering Models is a powerful simulation and modeling tool. TS4 is a file based simulation program, utilizing text files to simulate process steps, mask generation and photolithography and profile information. Physical processes are simulated numerically using the finite difference and finite element methods.

The structure is generated on a grid of non-overlapping triangular elements creating mesh nodes the total number of which must not exceed 20,000. Up to forty regions representing different materials can be represented including single crystal silicon, poly-silicon, silicon dioxide, silicon nitride, aluminum and photo resist. Prior to processing, the device structure must be specified using either automatic or manual grid generation or by reading structural information from external files. The structure is then initialized, specifying all relevant information including initial concentration of impurities and initial resistance, and crystalline orientation. Process steps that are simulated include material deposition, masking and photolithography, ion implantation, diffusion, Epitaxial growth and thermal oxidation each accompanied by parameters. Program output includes one and two-dimensional plots of a specified quantities, extraction of parameters and three-dimensional images of the simulated device. A slew of analytical and numerical models are also used to represent the diffusion of impurities and point defects, chemical predeposition, interstitial traps and carrier injection and recombination.

MEDICI is a device simulation program developed by Technology Modeling associates. In particular MEDICI can be used to analyze the behavior of a wide range of semiconductor device structures including the JFET, MOSFET, MESFET. Two dimensional carrier concentrations and potential contours, bias responses under transient conditions, analysis of deep sub-micron devices, I-V curve tracing and small AC signal analysis are among the simulations that can be performed.

3. STRUCTURAL CHARACTERISTICS

A. Structural Cross Section Results (NMOS Transistor)

Layer thickness and cross-section information serve as a primary characterization of the final structure under the ambient processing conditions. Table 1 represents the structural profile across the device through cross sections taken in the contact and gate regions respectively.

The values in the table are taken at bias voltages all set to 0 volts. The table depicts a junction depth in the contact region of approximately 0.56 μm . Simulation results encompass the device to a depth of 200 μm .

Profile for NMOS Transistor

Contact Area

Material	Thickness	Diffusion Type	Junction Depth
	μm		μm
Aluminum	0.6		
Silicon	0.392	N	0.56
	199.3937	P	200

Gate Area

Cap Oxide	0.08		
Polysilicon	0.45		
Oxide	0.0392		
Silicon	199.9766	P	200

Table 1. Structural Profile in Gate and Contact Regions for 2 μm NMOS Transistor

B. Structural Results (PMOS Transistor)

Profile for PMOS Transistor

Contact

Material	Thickness	Diffusion Type	Junction Depth
	μm		μm
Aluminum	0.6		
Silicon	0.3814	P	0.38
	2.0894	N	2.73
	196.9210	P	200

Gate

Polysilicon	0.45	P	0.45
Oxide	0.0387		
Silicon	0.01365	P	0.18
	2.3391	N	2.73
	197.0089	P	200

Table 2. Structural Profile in Gate and Contact Regions for 2 μm PMOS Transistor

Table 2 represents the structural profile across the device through cross sections taken in the contact and gate regions respectively for the PMOS Device. As the table depicts the cross section of the device is composed of a p-type channel

region implanted above a n-type well region implanted above the p-type silicon.

The values in the table are taken at bias voltages all set to 0 volts. The table depicts a junction depth in the contact region of approximately 0.38μm. The junction of the n-well and the substrate Simulation results encompass the device to a depth of 200μm.

C. Boron Threshold Implantation and Drive In

Figure 2 characterizes the concentration of Boron in the upper layers of the device immediately beneath the contact region. The graph depicts the significant increase in concentration of Boron as a result of the threshold voltage adjustment through the Ion Implantation step. An increased concentration of boron in the contact region increases the number of holes in the region thereby decreasing the threshold voltage of the majority carriers, electrons. The result of the LOCOS oxidation, indicated by the red line depicts a slight decrease in boron concentration at the oxide silicon interface of the device. After the Threshold implant however, the concentration of Boron under the oxide layer was significantly increased.

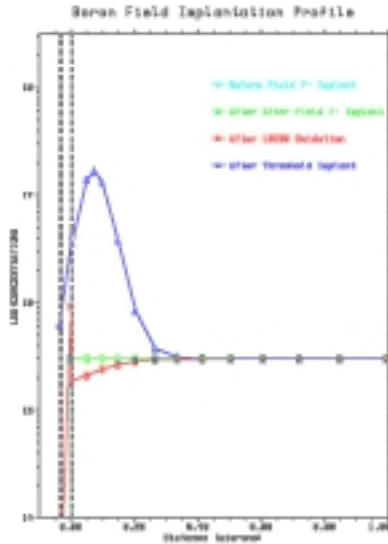


Figure 2. – Boron profile after the Threshold Ion Implantation and Field Drive In

D. Phosphorus Implantation Profiles

Figure 3 illustrates the effect of the ion implantation and drive in process on the phosphorus profile in the PMOS Transistor. The effect of the process on the location of the p-n junction is evidenced by noting the translation of the intersection of the phosphorus profile with that of the boron profile.

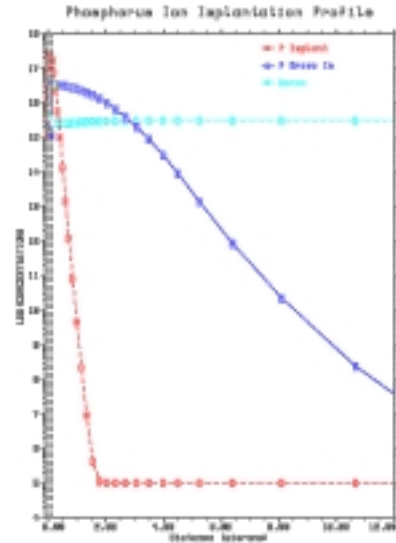


Figure 3. - Phosphorus Implantation and Drive in profiles for the N-Well.

4. THRESHOLD VOLTAGE

In demonstrating the relationships between the structural features of the device and the threshold voltage the simulations were carried out on a 20μm NMOS Transistor

The threshold voltage of operation of the device is determined from the plot of the drain source current voltage versus the gate voltage. The value is determined by extrapolation of the curve from the point of maximum slope to the x-axis intercept. The threshold voltage for the device is 0.461 volts at $V_{BS} = 0$ volts. The theoretical equation (1) for the threshold voltage of an ideal NMOS device is given by [3]

$$V_T = 2\phi_F + \frac{K_S x_O}{K_O} \sqrt{\frac{4qN_A}{K_S \epsilon_O} \phi_F} \quad (1)$$

The threshold voltage of the device is that gate voltage that induces an inversion channel under the oxide/silicon interface. The onset of inversion occurs at the point when the substrate surface potential (ϕ_S) is twice the magnitude of the reference potential related to the intrinsic doping concentration (ϕ_F). The first dashed red line indicates the inversion layer channel; the second red dashed line indicates the depletion layer, which increases in width as one moves from the source to the drain.

A. Threshold Voltage Variation with Substrate Voltage

Figure 4 depicts the simulation results for the effect of back biasing on the threshold voltage. These results were generated at $V_{DS}=0.1V$ and the substrate voltage ramped at 0.0, 2.5, and 5.0, 8.0 volts respectively. The corresponding threshold voltages were 0.461, 1.561, 2.266 and 3.310 volts respectively.

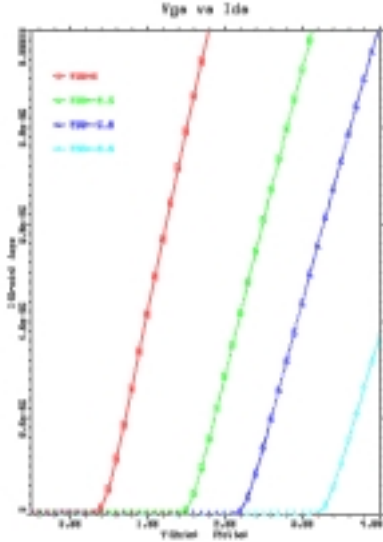


Figure 4. Drain current versus Gate voltage for four substrate bias potentials

B. Threshold Voltage variations with Oxide Thickness

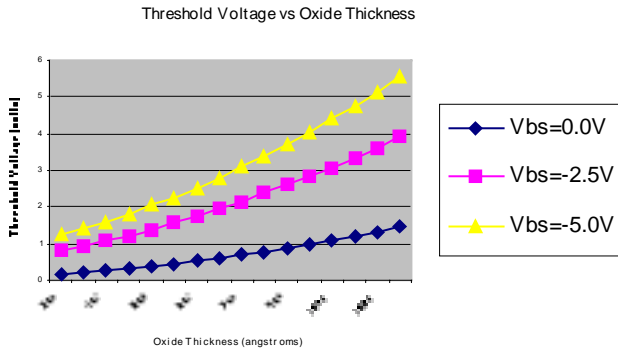


Figure 5. Threshold Voltage vs. Oxide Thickness for several substrate biases

I_{DS} was shown to be inversely related to the thickness of the gate oxide and as such the gate oxide will affect the threshold voltage of the device. Too thin an oxide induces current tunneling and the insulating qualities of the oxide are lost. Examining adjusting the gate oxidation temperature at a constant time length of 150 minutes modulated the thickness of the gate oxide. Assuming the gate

oxide is a perfect insulator then the gate voltage and the semiconductor surface potential are related by equation (2) [4]:

$$V_G = \phi_s + \frac{K_S}{K_O} x_o \sqrt{\frac{2qN_A}{K_S \epsilon_o}} \phi_s \quad (2)$$

Where ($0 \leq \phi_s \leq 2\phi_F$)

For gate oxide thickness in excess of 2000 Å the behavior departed from the linear model. In addition, increasing the gate oxidation temperature further beyond 2000 Å transitioned the device into depletion mode operation. This can be explained in terms of the gate area doping profiles. At higher gate oxidation temperatures lateral diffusion of phosphorus is increased. Thus there exists a point at which the p-n junction across the gate area makes contact and for $V_{GS} = 0$ a depletion layer already exists enabling conduction of a drain to source current. Figure 4., also demonstrates that the back biasing theory is supported across the range of oxide thickness from 300 Å to 1800 Å.

C. Threshold Voltage variations with Boron Concentration

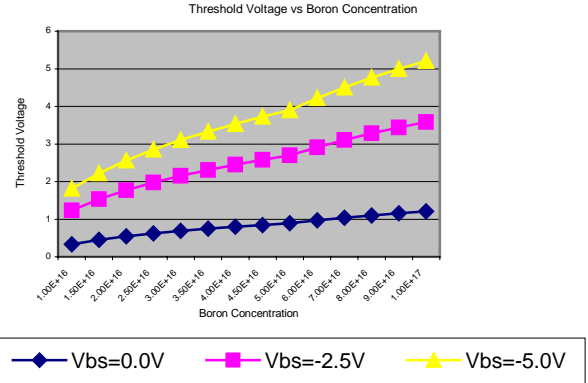


Figure 6. Threshold Voltage versus the initial Boron Concentration

Another parameter affecting the threshold voltage is the initial doping concentration of boron in the device. The process run for the device required an initial boron concentration of $1.55e^{16}$ atoms/cm³. The equation relating the threshold voltage to the initial boron concentration is given by:

$$V_T = \Phi_M - \chi - \frac{E_G}{2q} + |\Phi_F| + \frac{\sqrt{2K_S \epsilon_o q N_B (2|\Phi_F| + V_{BS})}}{C_0} - \frac{Q_{tot}}{C_0} \quad (3)$$

$$\text{Where: } |\Phi_F| = \left(\frac{kT}{q} \right) \ln \left(\frac{N_B}{n_i} \right)$$

Thus increasing the substrate doping, N_B causes an increase in the threshold voltage of the device. Simulations were performed, keeping all other quantities constant and changing the threshold voltage

An increased doping concentration in the structure at initialization means that there are more majority carriers under the oxide silicon interface in the gate region. As such, a higher concentration of minority carriers is needed to generate the inversion and depletion layers. However, since the initial concentration of phosphorus introduced into the structure remained constant then at the onset of conduction a larger threshold voltage would be been required.

5. I-V CURVE TRACES

The theoretical equation for the I-V curve trace is given by [5]:

$$I_D = \frac{Z\bar{\mu}_n C_o}{L} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \quad (4)$$

The pinch off voltage and corresponding saturation current for the device is given by the equation.

$$V_{Dsat} = V_G - V_T \quad (5)$$

$$I_{Dsat} = \frac{Z\bar{\mu}_n C_o}{2L} \left[(V_G - V_T)^2 \right] \quad (6)$$

The source, drain and gate electrodes being identified an I-V curve analysis was performed for gate voltages from zero to four at one volt intervals. Figure 7 illustrates the operation of the device in enhancement mode. The gate voltage determines the magnitude of the maximum conductance in the inversion layer channel. Once the threshold voltage has been met more minority carriers are drawn to the oxide silicon interface, the more minority carriers, the larger the maximum conductance of the channel and the larger the saturation current. Thus at a certain drain voltage the drain source current saturates. Increasing the gate voltage increases the drain source current through the inversion channel. It can also be inferred that at higher gate voltages the length of the inversion channel that is pinched off becomes comparable to the length of the channel. This is manifested in the fact that at higher gate biases, after the saturation gate voltage the drain source current continues to increase rather than being flat band. Figure 8 analyses the effect of the drain voltage on the I_{DS} vs. V_{GS} curve traces. As is expected for the same gate and substrate biases the larger the drain voltage, the larger the conductance in the inversion channels.

Figure 7 represents the characteristic IV characteristic for the NMOS transistor portion of the device. Drain current vs. drain voltage relationships was evaluated at several gate bias points of 10V, 8V, 6V, 4V, and 2V and at 0V gate bias. Increased gate voltages induce a larger number of majority carriers into the channel region thereby increasing the current at the saturation point of the device. Increased drain voltages on the device result in an increased current as more majority carriers are drawn into the drain region. Thus as the gate voltage increases the slope of the curve increases for larger drain voltages.

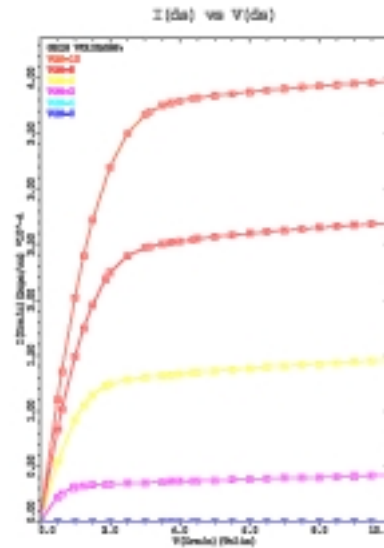


Figure 7. NMOS I-V Curve Trace

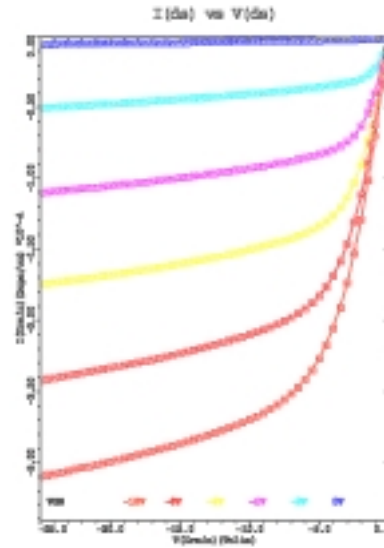


Figure 8. PMOS I-V Curve Trace

6. PROCESS PARAMETER RELATIONSHIPS

The final facet of the simulation of the Baseline involved deriving guidelines for the various processing parameters. The following charts illustrate the relationships concerned.

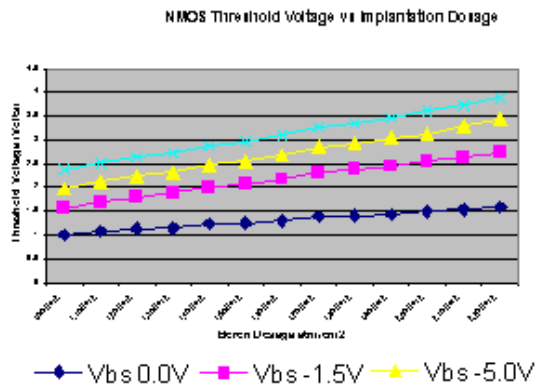


Figure 9. NMOS Threshold Voltage vs. Phosphorus Ion Implantation Dosage

The implantation dosage that is administered through determines the immediate concentration of Phosphorus Ions in the N-Well region of the device. As a result, an increased carrier concentration of n-type electrons requires more holes in the channels of the transistor in order to conduct a current.

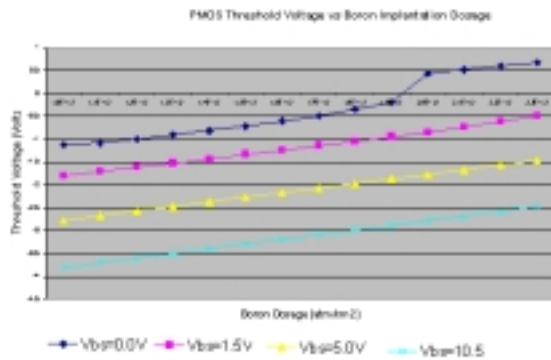


Figure 10. PMOS Threshold Voltage vs. Boron Implantation Dosage

Increasing the Boron Concentration in the P-type transistor has the same effect as increasing the Implantation Dosage as more holes are introduced into the substrate region of the device and as such a higher gate voltage is required to induce the critical number of carriers into the channel to cause inversion and conduct a current.

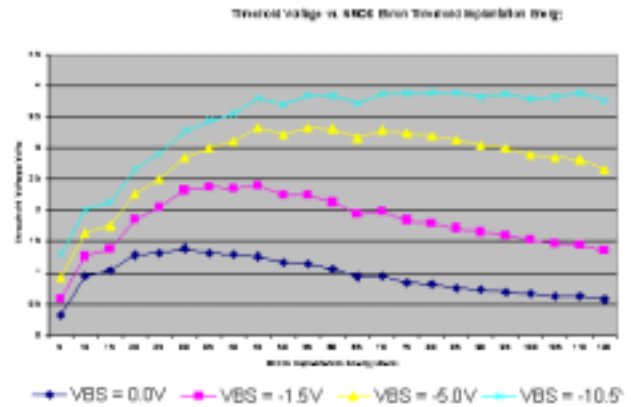


Figure 11. NMOS Threshold Voltage vs. Phosphorus Implantation Energy

Increasing the Boron Implantation Energy initially results in an increase in the Threshold Voltage owing to a more conducive distribution of Boron Carriers in the substrate. However, as this energy increase continues there is some breakdown of the voltage owing to the probable destruction of the structure of the substrate.

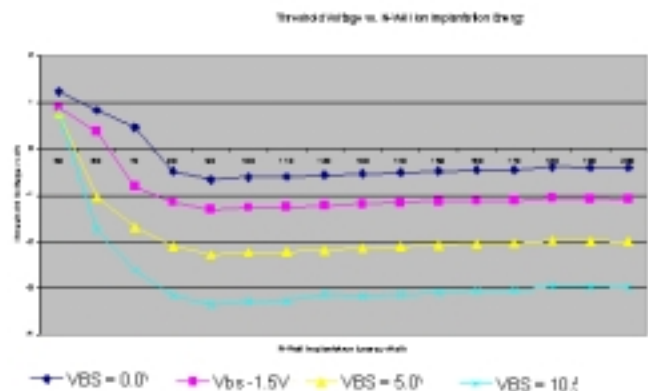


Figure 12. Threshold Voltage vs. N-Well Ion Implantation Energy.

7. CONCLUSION

This paper demonstrated the application of the process and device simulation software, TSUPREM-4 and MEDICI, to the CMOS Process Baseline at Georgia Institute of

Technology. In particular, the simulation tool was used to characterize the general relationships between process parameters and final device features.

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